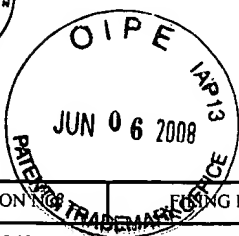




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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/633,869	08/07/2000	Hongyong Zhang	0756-2100	6768

7590 06/03/2008
Jeffrey L Costellia
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8180 Greensboro Drive
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McLean, VA 22102

EXAMINER

GHYKA, ALEXANDER G

ART UNIT	PAPER NUMBER
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2812

MAIL DATE	DELIVERY MODE
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06/03/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 09/633,869	Applicant(s) ZHANG ET AL.	
	Examiner ALEXANDER G. GHYKA	Art Unit 2812	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 August 2007.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) See Continuation Sheet is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☒ Claim(s) 31-36 and 67-70 is/are allowed.
6) ☒ Claim(s) 1,8,10,12,13,19,21,23,24,30-37,44,46,48,49,55,57,59,60 and 66-100 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 07 August 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Continuation of Disposition of Claims: Claims pending in the application are 1,8,10,12,13,19,21,23,24,30-37,44,46,48,49,55,57,59,60 and 66-100.

DETAILED ACTION

Applicants have indicated that the Final Rejection mailed 11/19/2007 has not been received. A copy of the Office action, as discussed below, is remailed. The response period is restarted.

Applicants' response of 8/31/2007 has been considered and entered in the record. New Claims 73-100 are added. Claims 1, 8, 10, 12-13, 19, 21, 23-24, 30, 31-36, 37, 44, 46, 48-49, 55, 57, 59-60 and 66-100 are under consideration. Claims 31-36 and 67-70 are allowed for the reasons as discussed below. New rejections are made in view of the Applicants' amendments.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 76, 83, 90 and 96 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no basis in the application as filed for the limitation "top gate type thin film transistor".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 10, 12, 13, 37, 46, 48-49 and 70-71 are rejected under 35 U.S.C. 102(e) as being anticipated by Chae (US 5,432,122).

The present Claims generally require a method for fabricating a semiconductor device having at least one thin film transistor comprising a channel region and a gate electrode, comprising the steps of: forming a semiconductor film comprising an amorphous silicon over a substrate; and irradiating said semiconductor film with a laser light along a scan direction, wherein said scan direction is parallel to said channel region.

With respect to Claims 1, 10, 37 and 46, Chae discloses a method of fabricating a semiconductor device having at least one thin film transistor comprising a channel region and a gate electrode, comprising the steps of: forming a structure comprising an amorphous semiconductor thin film separated by a gate insulating film from a gate electrode on an insulating substrate; irradiating said amorphous semiconducting film with a laser light to convert it to a polycrystalline film wherein said laser beam has a rectangular shaped cross section at said substrate, while relatively moving said laser beam along a scan direction across the substrate. See column 3, lines 45-68, and Figure 7. Moreover, Chae disclose the scanning direction is parallel to the channel region. See Figure 7.

With respect to Claims 12, 48 and 70, the irradiating step comprises moving the laser light in a scanning direction. See Figure 7.

With respect to Claims 13, 49, and 71, Chae et al disclose partially overlapping irradiation of the laser light. See column 6, lines 25-32.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 8, 18, 44 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chae (US 5,432,122) as applied to claims 1, 10, 12, 13, 37, 46, 48-49 above, and further in view of Imahashi et al (US 5,413,958).

Chae is relied upon as discussed above.

However, Chae does not disclose the use of the thin film transistor as a column driver (or source driver as referred to by the present Specification) or a scan driver (or a gate driver as referred to by the present Specification).

Imahashi et al disclose a method for manufacturing a liquid crystal display substrate, and disclose the use of a thin film transistor as a column driver or a scan driver. See column 2, lines 5-35.

It would have been obvious for one of ordinary skill in the art, at the time of the invention, to use the thin film transistor of Chae et al as a column driver or a scan driver, as Imahashi et al generally disclose the use of thin film transistors as column drivers or scan drivers. The use of a known device, thin film transistor, for its known utility, scan or column driver, would have been obvious to one of ordinary skill in the art in view of the cited references.

Claims 21, 23, 24, 57, 59, 60 and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chae (US 5,432,122) as applied to claims 1, 10, 12, 13, 37, 46, 48-49 above, and further in view of Weiner et al (US 5,565,377).

Chae is relied upon as discussed above.

However, Chae does not disclose implanting a dopant into the substrate before the laser irradiation.

Weiner et al disclose a process for forming retrograde and oscillatory profiles in crystalline and polycrystalline silicon. Weiner et al disclose implanting a dopant into the substrate before the laser irradiation. See Weiner et al, column 1, lines 18-22.

It would have been obvious to one of ordinary skill in the art to implant a dopant in the substrate of Chae before laser irradiation, for its known benefit of modifying the substrate as disclosed by the Weiner reference. As the introduction of dopants is known in the art of making semiconductors as disclosed by Weiner et al, a *prima facie* case of obviousness is established.

Claims 30 and 66 rejected under 35 U.S.C. 103(a) as being unpatentable over Chae (US 5,432,122) and Weiner et al (US 5,565,377) as applied to claims 21, 23, 24, 57, 59 and 60 above, and further in view of Imahashi et al (US 5,413,958).

Chae and Weiner et al are relied upon as discussed above.

However, Chae and Weiner et al do not disclose the use of the thin film transistor as a column driver (or source driver as referred to by the present Specification) or a scan driver (or a gate driver as referred to by the present Specification).

Imahashi et al disclose a method for manufacturing a liquid crystal display substrate, and disclose the use of a thin film transistor as a column driver or a scan driver. See column 2, lines 5-35.

It would have been obvious for one of ordinary skill in the art, at the time of the invention, to use the thin film transistor of Chae et al and Weiner et al as a column driver or a scan driver, as Imahashi et al generally disclose the use of thin film transistors as column drivers or scan drivers. The use of a known device, thin film transistor, for its known utility, scan or

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column driver, would have been obvious to one of ordinary skill in the art in view of the cited references.

New Rejection

Claims 73-100 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chae (US 5,432,122) and Weiner et al (US 5,565,377) as applied to claims 21, 23, 24, 57, 59 and 60 above, and further in view of Imahashi et al (US 5,413,958).

Chae and Weiner et al are relied upon as discussed above.

However, Chae and Weiner et al do not disclose the use of the thin film transistor as a column driver (or source driver as referred to by the present Specification) or a scan driver (or a gate driver as referred to by the present Specification).

Imahashi et al disclose a method for manufacturing a liquid crystal display substrate, and disclose the use of a thin film transistor as a column driver or a scan driver. See column 2, lines 5-35.

It would have been obvious for one of ordinary skill in the art, at the time of the invention, to use the thin film transistor of Chae et al and Weiner et al as a column driver or a scan driver, as Imahashi et al generally disclose the use of thin film transistors as column drivers or scan drivers. The use of a known device, thin film transistor, for its known utility, scan or column driver, would have been obvious to one of ordinary skill in the art in view of the cited references.

With respect to Claims 73-74, 79, 81 and 86, Weiner et al disclose a process for forming retrograde and oscillatory profiles in crystalline and polycrystalline silicon. Weiner et al disclose implanting a dopant into the substrate before the laser irradiation. See Weiner et al, column 1, lines 18-22.

With respect to Claim 75, 82, 89 and 95, Chae et al disclose a metal electrode. See Chae et al column 4, lines 58-62.

With respect to Claim 76, 83, 90 and 96, Chae et al disclose TFT transistors in general and encompass the present limitations.

With respect to Claims 77-78, 84, 85, 91, 92, 97 and 98, Chae et al disclose an excimer laser. See column 4, lines 55-59. The number of pulses would be a matter of optimization, which is well within the skill of one of ordinary skill in the art.

With respect to Claim 80, 87, 93 and 100, Chae et al disclose irradiating the electrode on the upper side. See Figure 7.

With respect to Claim 88 and 94, Weiner et al disclose a heating step. See the Abstract.

With respect to Claim 99, Imahashi et al disclose a method for manufacturing a liquid crystal display substrate, and disclose the use of a thin film transistor as a column driver or a scan driver. See column 2, lines 5-35.

Response to Applicants' Arguments

Applicants argue that Chae et al do not require "wherein said scan direction is parallel to said channel region". Applicants argue that the Chae reference discloses that the gate (22) extends along the scanning direction. See Figure 7. Applicants argue that the scanning direction of Chae is not parallel but perpendicular to the channel direction. In response to applicant's

argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., channel direction) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The present Claims call for a channel region, not channel direction. The Examiner notes that the present Claims are open through the use of the transitional phrase "comprising". The channel region is planar to the horizon, at least a portion of it. The scan direction is equidistant and planar to the horizon. Therefore, the scan direction is parallel to at least a portion of the channel. With respect to the rejections under 35 USC 103, Applicants argue that the secondary references do not cure the deficiencies of Chae. The Examiner maintains the rejections under 35 USC 103, for the reasons as discussed with respect to the rejection under 35 USC 102.

Allowable Subject Matter

Claims 31-36 and 67-70 are allowed.

The following is an examiner's statement of reasons for allowance: The cited prior does not anticipate or make obvious, *inter alia*, while relatively moving said energy beam along a scan which is orthogonal to the gate electrode and is parallel to the channel region, as required by the afore mentioned Claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

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fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander G. Ghyka whose telephone number is (571) 272-1669. The examiner can normally be reached on Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AGG
November 13, 2007

ALEXANDER G. GHYKA

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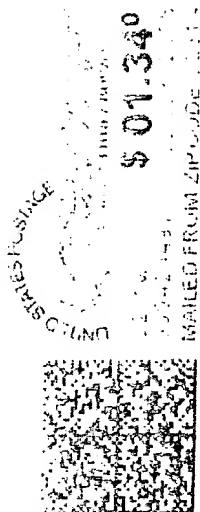
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